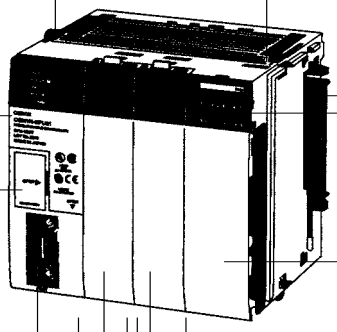
CPU Units

The four models of CPU Units can be broadly divided into two groups: Models that support Inner Boards and the Controller Link Unit, and models that do not. The CPU Units also vary in their program capacities, I/O capacities, memory capacities, and the presence of an RS-232C port, as shown in the *Basic Specifications* table, below.

■ NOMENCLATURE

The following illustration shows the main components of a CQM1H-CPU61 CPU Unit.



Sliders
Used to secure adjacent Units.

Battery Compartment Cover
Open this cover to access the battery, DIP switch, and Memory Cassette.

Connector
Add on Units horizontally by joining connectors.

LED indicators

Peripheral Port
Used to connect to Programming Devices such as a Programming Console or a computer running CX-Programmer. Also supports Host Link and no-protocol communications.

Built-in Inputs
There are 16 inputs built into CPU Unit.

RS-232C Port (except CQM1H-CPU11)
Used for Host Link, no-protocol, 1:1 Data Link, or NT link (1:1 mode) communications with external devices or other PLCs.

Inner Board Covers
Remove these covers when installing or removing Inner Boards.

Inner Board Slot 2 (right slot)
Use this slot to mount a High-speed Counter Board, Pulse I/O Board, Absolute Encoder Interface Board, Analog Setting Board, or Analog I/O Board.

Inner Board Slot 1 (left slot)
Use this slot to mount a High-speed Counter Board, Analog Setting Board, or Serial Communications Board.

■ OVERVIEW

Model	I/O capacity (See Note.)	Program capacity (words)	DM capacity (words)	EM capacity (words)	CPU Unit built-in inputs	Built-in serial ports		Inner Boards	Controller Link Module
						Peripheral port	RS-232C port		
CQM1H-CPU61	512	15.2 K	6 K	6 K	DC: 16	Yes	Yes	Supported	
CQM1H-CPU51		7.2 K	6 K	None					
CQM1H-CPU21	256	3.2 K	3 K					Not supported	
CQM1H-CPU11							No		

■ MAXIMUM NUMBER OF MODULES

CPU Unit	Controller Link Module	Inner Boards	I/O Modules and Dedicated I/O Modules
CQM1H-CPU61	1 max.	2 max.	11 max. 16 max. using I/O Expansion and Control Interface modules
CQM1H-CPU51			
CQM1H-CPU21	Not supported.	Not supported.	
CQM1H-CPU11			

Note: I/O capacity = Number of input points (≤ 256) + Number of output points (≤ 256).

■ CPU UNIT SPECIFICATIONS

Characteristics

Item		Specifications
Control method		Stored program method
I/O control method		Cyclic scan and direct output/immediate interrupt processing
Programming language		Ladder-diagram programming
I/O capacity		CQM1H-CPU11/21: 256 CQM1H-CPU51/61: 512
Program capacity		CQM1H-CPU11/21 : 3.2 kwords CQM1H-CPU51 : 7.2 kwords CQM1H-CPU61 : 15.2 kwords
User data memory capacity		CQM1H-CPU11/21 : 3 kwords CQM1H-CPU51 : 6 kwords CQM1H-CPU61 : 12 kwords (DM: 6 kwords; EM: 6 kwords)
Instruction length		1 step per instruction, 1 to 4 words per instruction
Number of instructions		162 (14 basic, 148 special instructions)
Instruction execution times		Basic instructions: 0.375 to 1.125 μs Special instructions: 17.7 μs (MOV instruction)
Overseeing time		0.70 ms
Mounting structure		No backplane (Modules are joined horizontally using connectors)
Mounting		DIN Track mounting (screw mounting not possible)
CPU Unit built-in DC input points		16
Maximum number of modules		Maximum of 11 modules total for I/O modules and Dedicated I/O modules
Inner Boards		CQM1H-CPU11/21: None CQM1H-CPU51/61: 2 Boards
Communications modules (Controller Link Module)		CQM1H-CPU11/21: None CQM1H-CPU51/61: 1 module
Types of interrupts	Input interrupts (4 inputs max.)	Input Interrupt Mode: Interrupts are executed in response to inputs from external sources to the CPU Unit's built-in input points. Counter Mode: Interrupts are executed in response to reception of a set number of pulses (counted down) via the CPU Unit's internal built-in input points (4 points).
	Interval timer interrupts (3 timers max.)	Scheduled Interrupt Mode: Program is interrupted at regular intervals measured by one of the CPU Unit's internal timers. One-shot Interrupt Mode: An interrupt is executed after a set time, measured by one of the CPU Unit's internal timers.
	High-speed counter interrupts	Target Value Comparison: Interrupt is executed when the high-speed counter PV is equal to a specified value. Range Comparison: Interrupt is executed when the high-speed counter PV lies within a specified range. Counting is possible for high-speed counter inputs from the CPU Unit's internal input points, Pulse I/O Boards, or Absolute Encoder Interface Boards. (The High-speed Counter Board has no interrupt function, but can output bit patterns internally and externally.)
I/O allocations		I/O is automatically allocated in order from the Unit nearest to the CPU Unit. (Because there are no I/O tables, it is not necessary to create I/O tables from a Programming Device.)